REMARKS

Please reconsider the application in view of the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1, 3-6, 18, 19 and 23-27 are pending in the application. Claims 1, 18, and 19 are independent. The remaining claims depend, directly or indirectly, from claims 1 and 19.

II. Rejection(s) under 35 U.S.C §103

Claims 1, 3-6, 18, 19, and 23-27 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,483,361 issued to Chiu (hereinafter "Chiu") in view of U.S. Patent No. 6,496,554 issued to Ahn (hereinafter "Ahn"). For the reasons listed below, this rejection is respectfully traversed.

The Present Invention

The present invention relates to a technique for detecting whether a phase locked loop is out of lock. As recited in claim 19, a method of the present invention includes generating a first signal and a second signal based on a relationship between a system clock and a chip clock used in a phase locked loop. In particular, the first and second signals are generated by a phase frequency detector in the phase locked loop. The method further includes determining whether a pulse of the first signal or the second signal is greater than a predetermined width and generating a pulse on a first lock signal, based on the determination. The method also includes generating a pulse on a lock status

signal, which is dependent on the first lock signal.

For example, as shown in the exemplary embodiment of the present invention shown in Figure 3, the phase frequency detector (44) inputs a system clock (sys_clk) and a chip clock (chip_clk) and outputs a fast signal (fast_pulse) and a slow signal (slow_pulse). A lock detect indicator (42) of the present invention inputs the fast signal (fast_pulse), the slow signal (slow_pulse), the system clock (sys_clk), and chip clock (chip_clk) and generates a lock status signal (lock_status), which indicates whether the phase locked loop is in (or out of) lock. More particularly, determining whether the phase locked loop is in (or out of) lock is based on a pulse width of the fast (fast_pulse) or slow signal (slow_pulse) being greater than a predetermined width. (*See* specification pp. 5 and 6.) The Applicant notes that independent claims 1, 18, and 19 require, at least in part, a predetermined pulse width.

The Present Invention v. Chiu & Ahn

Chiu and Ahn fail to render the present invention obvious, because the combination of Chiu and Ahn is improper. In particular, there is no reasonable expectation of success of the combination of the references. Chiu teaches a lock detector circuit, which determines whether a phase locked loop is in (or out of) lock based on a *phase difference* between up and down signals. On the other hand, the present invention determines whether a phase lock loop is in (or out of) lock based on a *pulse width* of a first or a second signal (*e.g.*, a fast or a slow signal) being greater than a predetermined pulse width. As acknowledged by the Examiner, Chiu fails to teach a lock detector circuit that uses a pulse width of a first or a second signal to determine whether the phase locked loop is in (or out of) lock.

Ahn has been combined with Chiu to purportedly provide that which Chiu lacks, namely, using pulse widths of the first or second signals. However, Ahn explicitly denigrates the use of pulse widths of the first and second signals. For example, Ahn states, "[u]nfortunately, the pulse widths of the up and down control signals are subject to temperature and process variation and therefore are not well suited as control parameters for ascertaining phase lock," (col. 1, ll. 48-51). In other words, Ahn asserts that pulse widths should *not* be used in determining whether a phase locked loop is in (or out of) lock. With respect to the alleged inaccuracy of pulse widths, Ahn continues, "[t]he pulse widths of up and down control signals are merely rough indicators having limited accuracy of the true phase relationship between the input signals of the phase detector," (col. 1, ll. 51-54). To overcome these purported inaccuracies, Ahn teaches using a window signal generating circuit, rather than using a pulse width of the up and down control signals.

In order to establish a case of *prima facie* obviousness, (1) the combination of the references must teach all of the elements of the present invention; (2) there must be a motivation to combine the references; and (3) there must be a reasonable expectation of success of the combination. The Examiner cannot combine prior art references to render a claimed invention obvious by merely showing that all the limitations of the claimed invention can be found in the prior art references. Instead, there must a suggestion or motivation to combine the references within the prior art references themselves. In other words, regardless of whether prior art references can be combined, there must an indication within the prior art references *expressing desirability* to combine the references. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). Further, the present application

cannot be used a guide in reconstructing elements of prior art references to render the claimed invention obvious. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added).

Furthermore, with respect to the success of the combination, Ahn clearly indicates that there is no expectation of success from using pulse widths of up and down signals. Recall, Ahn states, "the pulse widths...are not well suited from ascertaining phase lock." Because Ahn teaches that using the pulse widths of up and down control signals are inaccurate, there *cannot* be a reasonable expectation of success of the combination of Chiu and Ahn, as required to establish a *prima facie* case of obviousness. Therefore, the combination of Chiu and Ahn is improper and claims 1, 18, and 19 are patentable over the combination of Chiu and Ahn. Claims 3-6 and 23-27, being dependent on claims 1 and 19, are likewise patentable for at least the same reasons.

III. Conclusion

The above remarks are believed to require no further prior art search. Also, Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Because the remarks simplify the issues for allowance or appeal, and do not constitute new matter, entry and consideration thereof is respectfully requested. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.139001).

Respectfully submitted,

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